National Semiconductor

February 19, 2008

LM3487
High Efficiency High-Side N-Channel Controller for Switching Regulator

General Description

The LM3487 is a high-side N-channel MOSFET switching regulator controller. It can be used in topologies requiring a high side MOSFET such as buck, inverting (buck-boost) and zeta regulators. The LM3487's internal push pull driver allows compatibility with a wide range of MOSFETs. A wide input voltage range and an adjustable current limit allow the LM3487 to be optimized for a wide variety of applications.

The LM3487 has an adjustable switching frequency which can also be synchronized to an external clock. Current-mode control requires only a single resistor and capacitor for frequency compensation. The current mode architecture also yields superior line and load regulation and cycle-by-cycle current limiting. A 7µA shutdown state can be used for power savings and for power supply sequencing. Other features include external soft-start to reduce inrush current and output over voltage protection.

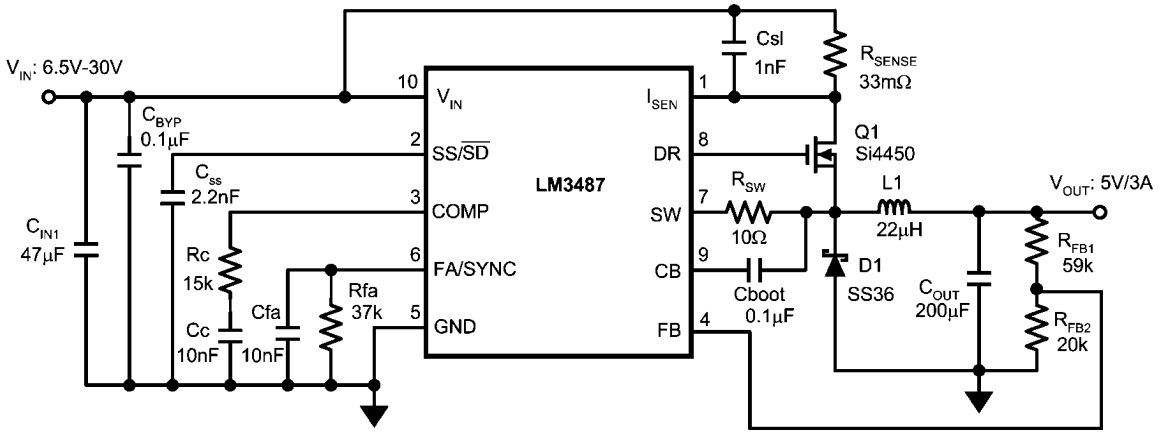
Features

- Adjustable/synchronizable switching frequency from 100kHz to 1.4MHz
- Adjustable cycle by cycle current limit
- Wide 3V-35V input voltage range
- Thermal shutdown
- Frequency compensation optimized with a single capacitor and resistor
- External softstart
- Current mode operation
- Undervoltage lockout with hysteresis
- 10-lead Mini-SO10 (MSOP-10) package
- Automotive grade including AEC-Q100 is available

Applications

- ADSL Modems
- Local Voltage Regulation
- Distributed Power
- Notebook and Palmtop Computers
- Internet Appliances
- Printers and Office Automation
- Battery operated Devices
- Cable Modems
- Battery Chargers

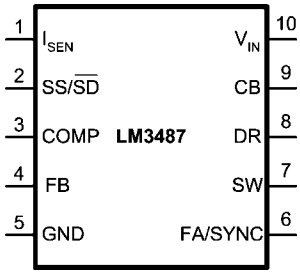
Typical Application Circuit



Typical High Efficiency Step-Down (Buck) Converter

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Connection Diagram



20049202

10-Lead Mini SO10 Package (MSOP-10 Package)

Package Marking and Ordering Information

Order Number	Package Type	Package Marking	Supplied As:
LM3487MM	MSOP-10	S38B	1000 units on Tape and Reel
LM3487MMX			3500 units on Tape and Reel
LM3487QMM			1000 units on Tape and Reel
LM3487QMMX			3500 units on Tape and Reel

For automotive grade including AEC-Q100 use 'Q' versions.

Pin Descriptions

Pin Name	Pin Number	Description
ISEN	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
SS/$\overline{SD}$	2	Soft-Start and Shutdown pin. Connect a capacitor from this pin to ground to achieve soft-start. Pull this pin below 0.7V (typical) to shutdown the device.
COMP	3	Compensation pin. A resistor-capacitor combination connected to this pin provides compensation for the control loop.
FB	4	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.260V (typical) at this pin.
GND	5	Ground pin.
FA/SYNC	6	Frequency adjust and synchronization pin. Connect a resistor from this pin to ground to set the switching frequency. Connect a high impedance clock signal to this pin to synchronize the switching frequency with the rising edge of the clock.
SW	7	Switch Node. Source of the external MOSFET is connected to this node.
DR	8	Drive pin. The gate of the external MOSFET should be connected to this pin.
CB	9	Boot-strap pin. A capacitor must be connected between this pin and SW pin (pin 5) for proper operation. The voltage developed across this capacitor provides the gate drive for the external MOSFET.
VIN	10	Power Supply Input pin.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN (Note 2)	45V
Peak Driver Output Current (<10ns)	1.0A
FA/SYNC	5.5V
SW	VIN
FB	2.5V
CB	7.2V + V_{SW}
ISEN	(Vin-500mV) to Vin
Power Dissipation (Note 3)	.5W
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
ESD Susceptibility (Note 4)	
Human Body Model	2kV
Machine Model	200V
Lead Temperature for MSOP Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Note 1)

Supply Voltage	2.97V ≤ V_{IN} ≤ 35V
Junction Temperature Range	−40°C ≤ T_J ≤ +125°C

Electrical Characteristics (Note 5)

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V.

Symbol	Parameter	Conditions	Typical	Limit	Units
V_{FB}	Feedback Voltage	V_{comp} = 0.7V	1.260	**1.210** **1.290**	V V(min) V(max)
ΔV_{LINE}	Feedback Voltage Line Regulation	2.97V ≤ V_{IN} ≤ 35V	0.001		%/V
ΔV_{LOAD}	Output Voltage Load Regulation		±0.5		%/V (max)
V_{UVLO}	Input Undervoltage Lock-out		2.80	**2.97**	V V(max)
$V_{UVLO(HYS)}$	Input Undervoltage Lock-out Hysteresis		180	**100** **235**	mV mV (min) mV (max)
F_S	Nominal Maximum Switching Frequency	R_{FA} = 9.76K	1.45	**1.25** **1.66**	MHz MHz(min) MHz(max)
R_{DRIVE}	Driver Switch On Resistance (Source)	I_{DR} = 0.2A, V_{IN}= 5V	7		Ω
R_{DRIVE}	Driver Switch On Resistance (Sink)	I_{DR} = 0.2A	9		Ω
D_{max}	Maximum Duty Cycle (Note 6)		100		%
T_{min} (on)	Minimum On Time		130		nsec
I_{SUPPLY}	Supply Current (switching)	SS/$\overline{SD}$=open DR=open	2.4	**6**	mA mA (max)
I_Q	Quiescent Current in Shutdown Mode	V_{IN} = 5V, SS/$\overline{SD}$=0V	7.3	**10**	µA µA (max)
$V_{CL(O)}$	Current Limit Voltage at 0% Duty Cycle	V_{IN} = 5V	155	**90** **200**	mV mV (min) mV (max)
$V_{CL(100)}$	Current Limit Voltage at 100% Duty Cycle	V_{IN} = 5V	118	**60** **120**	mV mV (min) mV (max)
V_{SC}	Short-Circuit Current Limit Sense Voltage	V_{IN} = 5V	350	**270** **420**	mV mV (min) mV (max)
V_{SL}	Internal Compensation Ramp Voltage Height	V_{IN} = 5V	65		mV
V_{OVP}	Output Over-voltage Protection (with respect to feedback voltage) (Note 7)	V_{COMP} = 0.7V	50	**40** **110**	mV mV(min) mV(max)

Symbol	Parameter	Conditions	Typical	Limit	Units
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis(Note 7)	V_{COMP} = 0.7V	60	 **20** **110**	mV mV(min) mV(max)
Gm	Error Amplifier Transconductance	V_{COMP} = 0.7V	750	 500/**300** 1000/**1300**	µmho µmho (min) µmho (max)
I_{EAO}	Error Amplifier Output Current (Source/ Sink)	Source, V_{COMP} = 0.7V, V_{FB} = 0V	103		µA
		Sink, V_{COMP} = 0.7V, V_{FB} = 1.4V	138		µA
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit V_{FB} = 0V COMP Pin = Floating	1.5		V V(min) V(max)
		Lower Limit V_{FB} = 1.4V	0.4		V V(min) V(max)
V_{SD}	Shutdown Threshold (Note 8)		0.7		V
V_{SYNC}	FA/SYNC Threshold Voltage		2.5		V
I_{SS}	SS Source Current	V_{SD} = 0V	2.4		µA
TSD	Thermal Shutdown		165		°C
T_{SH}	Thermal Shutdown Hysteresis		10		°C
θ_{JA}	Thermal Resistance	MM Package	200		°C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The Absolute Maximum V_{IN} rating of 45V is for non-operational (storage) conditions only. The maximum operating voltage is 35V.

Note 3: The maximum allowable power dissipation is calculated by using $PD_{MAX}= (T_{JMAX}-T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance of the package. The 0.5W rating results from using 125°C, 25°C, and 200°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 200°C/W represents the worst case condition of no heat sinking of the MSOP-10 package.

Note 4: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is 200 pF capacitor discharged directly into each pin.

Note 5: All limits are guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 6: 100% duty cycle can be achieved only for a limited number of cycles before the CB voltage collapses and the device shuts down.

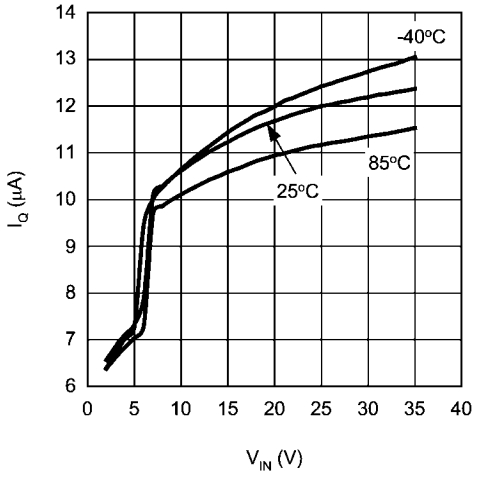
Note 7: The over-voltage protection is specified with respect to the feedback voltage. The overvoltage protection threshold is given by adding the feedback voltage, V_{FB} to the over-voltage protection specification.

Note 8: The SS/$\overline{SD}$ pin must be pulled below this limit to turn the regulator off.

Typical Performance Characteristics

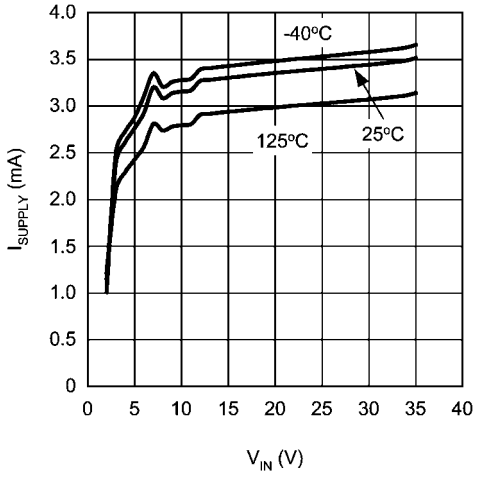
Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

I_Q (Shutdown) vs Temperature & Supply Voltage



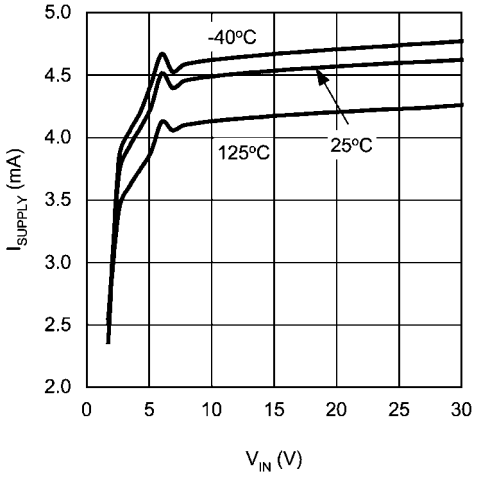
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I_{Supply} vs Temperature & Supply Voltage (Non-Switching)



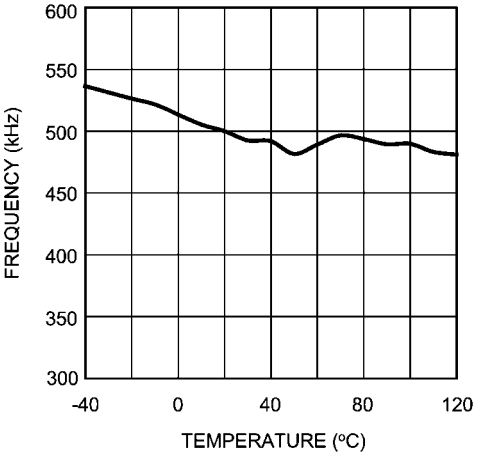
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I_{Supply} vs Temperature & Supply Voltage (Switching)



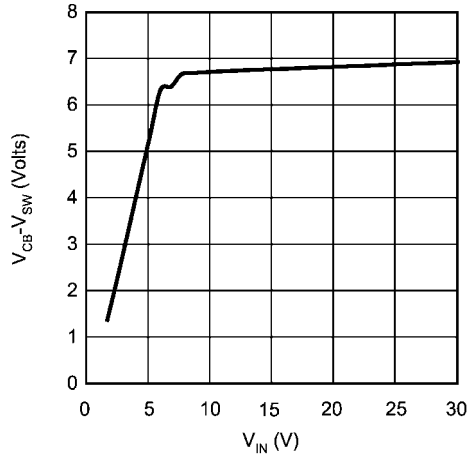
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Frequency vs Temperature



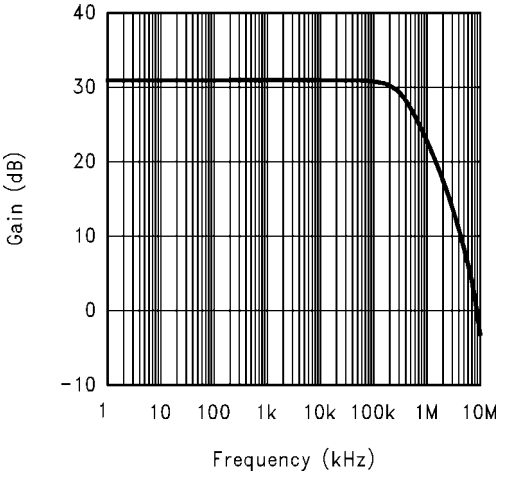
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V_{CB}–V_{SW} vs Supply Voltage



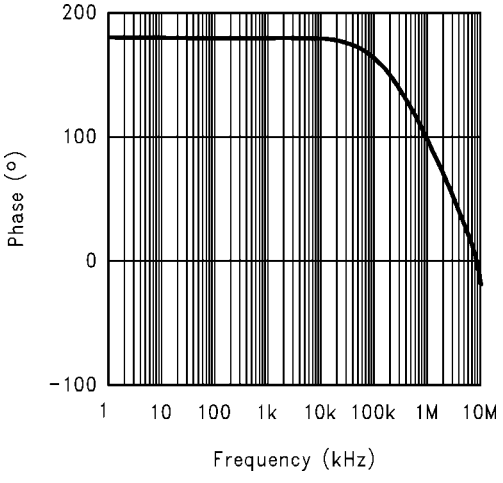
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Error Amplifier Gain



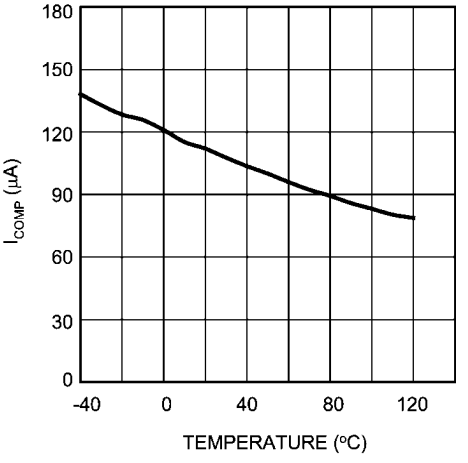
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Error Amplifier Phase Shift



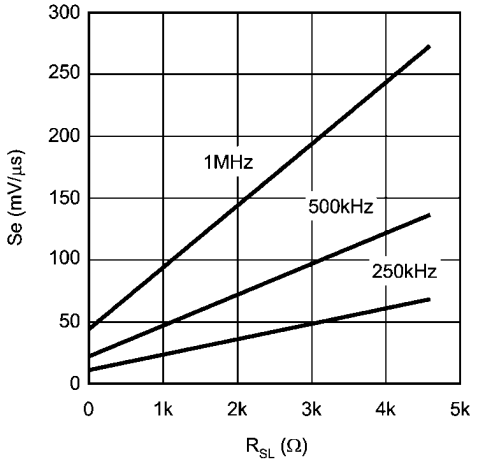
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COMP Pin Source Current vs Temperature



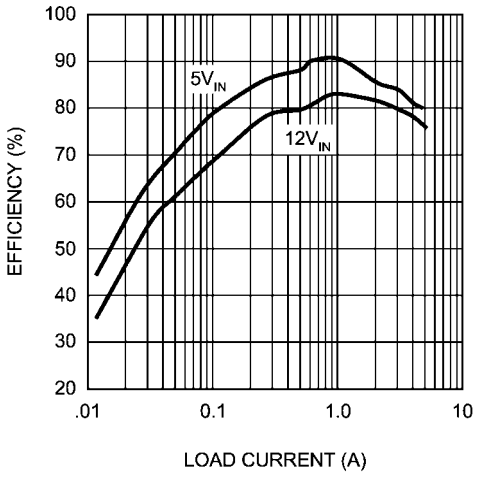
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Slope Compensation Ramp vs Slope Compensation Resistor



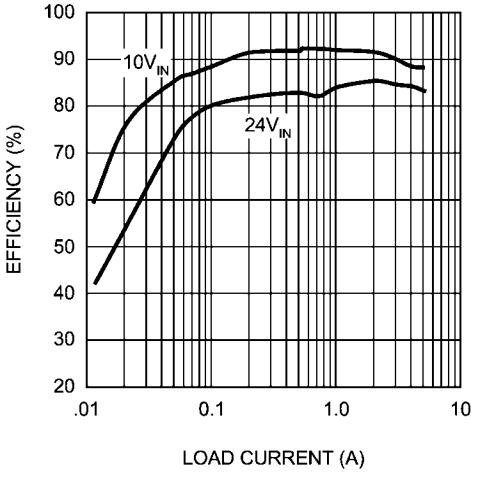
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Efficiency vs Load Current (V_{OUT} = 2.5V, 500kHz)



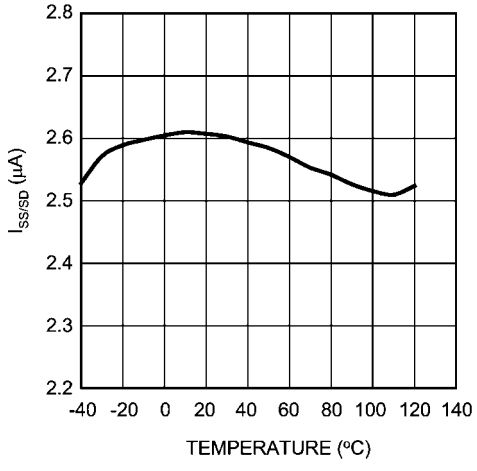
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Efficiency vs Load Current (V_{OUT} = 5V, 500kHz)



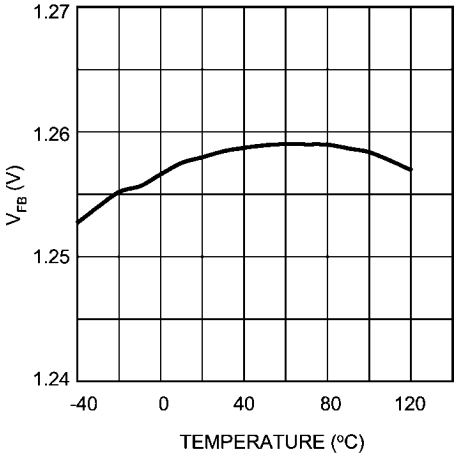
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Softstart Source Current vs Temperature



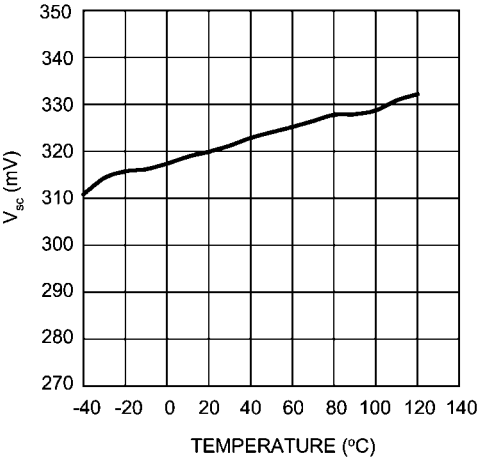
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V_{FB} vs Temperature



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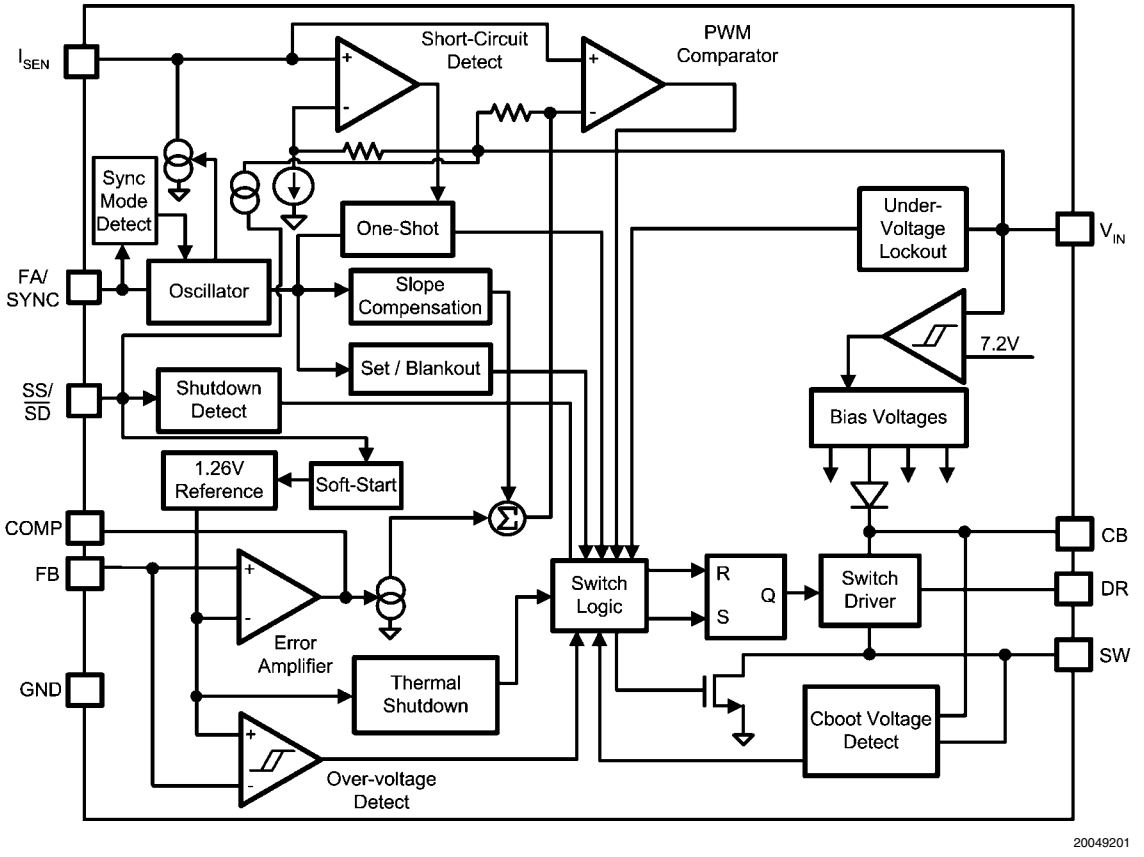
Short Circuit Threshold Voltage vs Temperature



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Functional Description

Functional Block Diagram



GENERAL DESCRIPTION

The LM3487 is a switching regulator controller for topologies incorporating a high side switch. The most common of these topologies is the step-down, or buck, converter. Other topologies such as the inverting (buck-boost) and inverse SEPIC (zeta) converters can also be realized. This datasheet will focus on buck converter applications.

The LM3487 employs current mode control architecture. Among the many benefits of this architecture are superior line and load regulation, cycle-by-cycle current limiting, and simple loop compensation. A patented adjustable slope compensation scheme enables flexible inductor selection. The LM3487 has a combination of features that allow its use in a wide variety of applications. The input voltage can range from 2.97V to 35V, with the output voltage being positive or negative depending on the topology. The current limit can be scaled to safely drive a wide range of loads. An external soft-start is used to limit initial in-rush current. Output over voltage and input under voltage protection ensure safe operation of the LM3487.

REGIONS OF OPERATION

Pulse width modulation (PWM) is the normal mode of operation. In PWM, the output voltage is well regulated and has a ripple frequency equal to the switching frequency. In low load conditions, the part operates in hysteretic mode. In this mode, the output voltage is regulated between a high and low value that results in a higher ripple magnitude and lower ripple frequency than in PWM mode (see *OVER VOLTAGE PROTECTION* section).

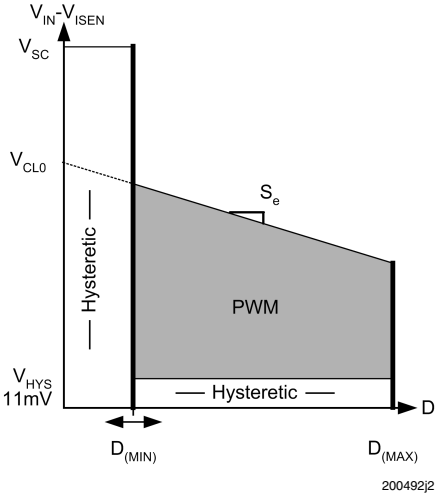


FIGURE 1. Operating Regions of the LM3487

Figure 1 shows the operating regions of the LM3487. The device will enter hysteretic mode below minimum duty cycle, or at low loads below the V_{HYS} threshold. Above the V_{CL} threshold, the device is in current limit. V_{SC} is the current limit ceiling.

Above this ceiling, the device enters short circuit protection mode (see the *SHORT CIRCUIT CURRENT LIMIT* section).

The voltages in *Figure 1* can be referred to the switch current by dividing through by R_{SN}. The LM3487 has a low hysteretic threshold voltage V_{HYS}, and thus will operate in PWM mode for a large load range. Typically, V_{HYS} = 11mV for the LM3487.

FREQUENCY ADJUST/SYNCHRONIZATION

The switching frequency of the LM3487 can be adjusted between 100kHz and 1.4MHz using a single external resistor. This resistor must be connected from FA/SYNC pin to ground as shown in *Figure 2*. See *Figure 3* to determine the required resistance to set a switching frequency. To ensure stable operation, a 10nF capacitor should be placed in parallel with the resistor as shown. The LM3487's switching frequency can also be synchronized to an external signal. A switching period is initialized at every rising edge of the applied external signal. The synchronizing signal should transition between 0V and at least 2.5V, but no greater than 5.5V. The signal must have a pulse width of at least 100 ns.

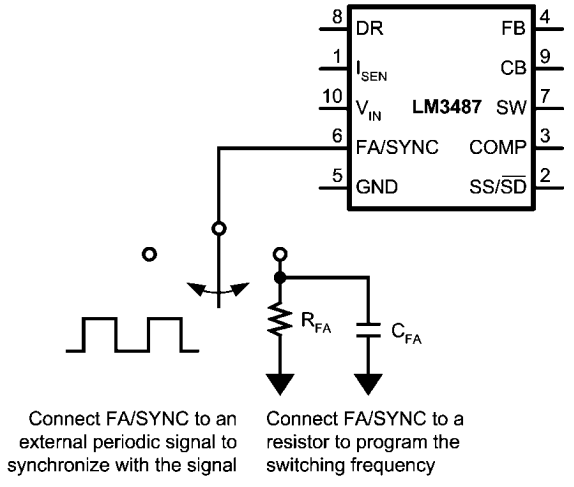


FIGURE 2. Programming the Switching Frequency

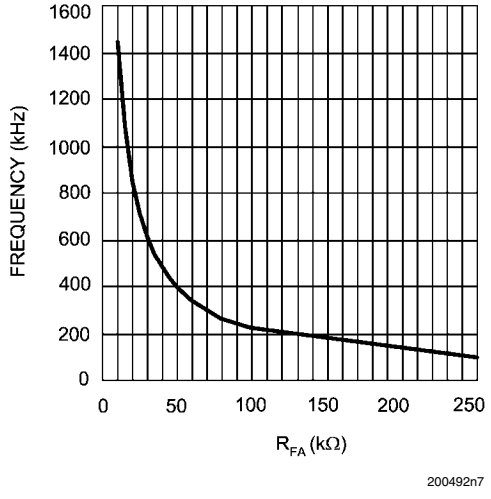


FIGURE 3. Frequency vs R_{FA}

OVER VOLTAGE PROTECTION

The LM3487 has over voltage protection (OVP) for the output voltage. OVP is sensed at and is in respect to the feedback pin (pin 4). If at anytime the voltage at the feedback pin rises to V_{FB} + V_{OVP}, OVP is triggered. See *ELECTRICAL CHARACTERISTICS* section for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3487 will begin switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See *ELECTRICAL CHARACTERISTICS* for limits on $V_{OVP(HYS)}$.

OVP can be triggered by any event that causes the output voltage to rise out of regulation. There are several common circumstances in which this can happen, and it is beneficial for a designer to be aware of these for debugging purposes, since the mode of operation changes from the normal Pulse Width Modulation (PWM) mode to the hysteretic mode. In the hysteretic mode the output voltage is regulated within the OVP hysteresis window, which results in a higher ripple magnitude and lower ripple frequency than in the PWM mode, see *Figure 4*.

It is useful to plot the operational boundaries in order to illustrate the point at which the device switches into hysteretic mode. In *Figure 4*, the limits shown are with respect to the peak voltage across the sense resistor R_{SEN}, (V_{SENpk}); they can be referred to the peak inductor current by dividing through by R_{SEN}. In normal circumstances V_{SENpk} is within the shaded region, and the LM3487 will operate in the PWM mode. If operating conditions are chosen such that V_{SENpk} would not normally fall in the shaded regions (for example, under light load), then the mode of operation is changed so that V_{SENpk} will be forced into the shaded region, and the part will operate in the hysteretic mode. The LM3487 will not allow V_{SENpk} to be outside of the shaded regions, so the duty cycle is adjusted accordingly.

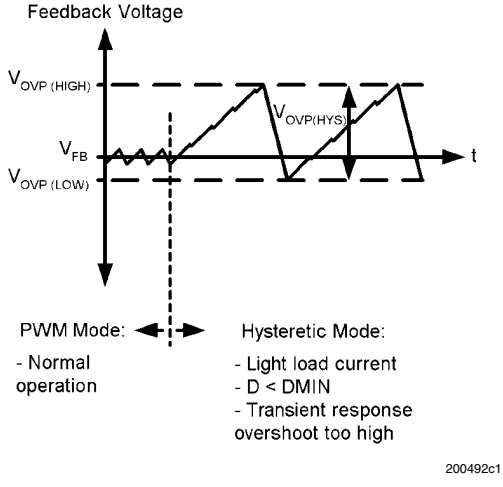


FIGURE 4. The Feedback Voltage is related to the Output Voltage. See different Ripple Components in PWM and Hysteretic Modes

If the load current becomes too low, and V_{SENpk} falls below V_{HYS}, the LM3487 will increase the duty cycle, causing the voltage to rise and trigger the OVP.

Another way OVP can be tripped is if the input voltage rises higher than the LM3487 is able to regulate in pulse width modulation (PWM) mode. The output voltage is related to the input voltage by the duty cycle as: V_{OUT} = V_{IN}*D. Minimum

duty cycle can be calculated as $D_{MIN} = T_{ON(MIN)} * f_{SW}$. Where $T_{ON(MIN)}$ is the minimum on time of 130ns (typical). If the input voltage increases such that the duty cycle wants to be less than D_{MIN}, the duty cycle will hold at D_{MIN} and the output voltage will increase with the input voltage until it trips OVP.

An output voltage transient response overshoot can also trigger OVP. As discussed in the *OUTPUT CAPACITOR* section, if the capacitance is too low or ESR too high, the output voltage overshoot can rise high enough to trigger OVP. However, as long as there is room for the duty cycle to adjust (the converter is not near D_{MIN} or D_{MAX}), the LM3487 will return to PWM mode after a few cycles of hysteretic mode operation.

There is one last way that OVP can be triggered. If the unregulated input voltage crosses 7.2V, the output voltage will react as shown in *Figure 5*. The internal bias of the LM3487 switches on at 7.2V input. When this happens, a sudden small change in bias voltage is seen by all the internal blocks of the LM3487. The control voltage, VC, shifts because of the bias change, and the PWM comparator tries to keep regulation. To the PWM comparator, the scenario is identical to a step change in the load current, so the response at the output voltage is the same as would be observed in a step load change. Hence, the output voltage overshoot here can also trigger OVP. The LM3487 will regulate in hysteretic mode for several cycles, or may not recover and simply stay in hysteretic mode until the load current drops. Note that the output voltage is still regulated in hysteric mode. Predicting whether or not the LM3487 will come out of hysteretic mode in this scenario is a difficult task, however it is largely a function of the output current and the output capacitance. Triggering hysteretic mode in this way is only possible at higher load currents. To avoid this condition, increase the output capacitance.

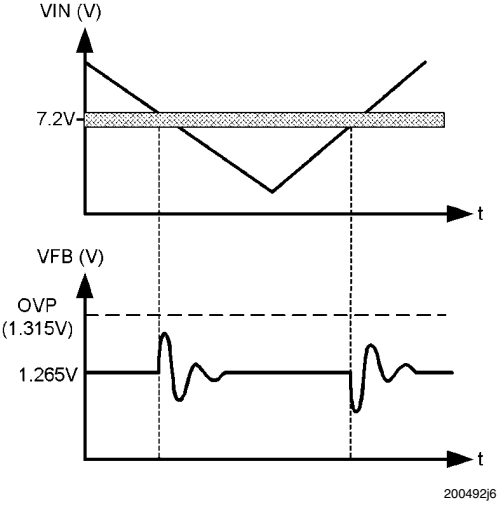


FIGURE 5. The Feedback Voltage Experiences an Oscillation if the Input Voltage Crosses the 7.2V Internal Bias Threshold

DEFAULT/ADJUSTABLE SLOPE COMPENSATION

The LM3487 uses a current mode control scheme. There are many advantages in a current mode architecture including inherent cycle-by-cycle current limiting and simple compensation of the control loop. However, there are consequences to using current mode control that one must be aware of while selecting circuit components. One of these consequences is the inherent possibility of subharmonic oscillations in the inductor current. This is a form of instability and should be avoided.

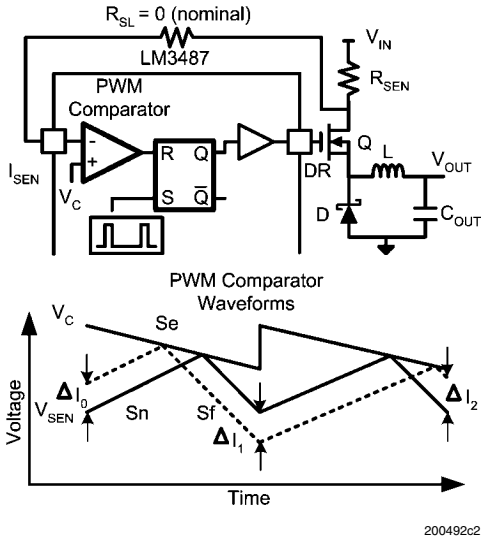


FIGURE 6. The Current Sensing Loop and Corresponding Waveforms

As a brief explanation, consider *Figure 6*. The top portion shows a schematic of the current sensing loop. The bottom portion shows the pulse width modulation (PWM) comparator waveforms for two switching cycles. The two solid waveforms shown are the waveforms compared at the internal pulse width modulator, used to generate the MOSFET drive signal. The top waveform with the slope S_e is the internally generated control waveform V_C. The bottom waveform with slopes S_n and S_f is the sensed inductor current waveform V_{SEN}. V_{SEN} is fed back to the PWM comparator, where it is compared to V_C. The output of the comparator in combination with the R/S latch determine if the MOSFET is on or off, which effectively controls the amount of current the inductor receives. While V_C is higher than V_{SEN}, the PWM comparator outputs a high signal, driving the external power MOSFET on. When MOSFET is on, the inductor current rises at a constant slope, generating the sensed voltage V_{SEN}. When V_{SEN} equals V_C, the PWM comparator turns the MOSFET off, and the sensed inductor current decreases with a slope S_f. The process begins again when R_S latch is set by an internal oscillator.

The subharmonic oscillation phenomenon occurs when a load excursion is experienced. It is analyzed by calculating how the inductor current settles after such an excursion. Take for example the case when the inductor current experiences a step increase in its average current, shown as the dotted line in *Figure 6*. In the switching period that the excursion occurs, the inductor current will change by ΔI_0. In the following switching period, the inductor current will have a difference ΔI_1 from its original starting value. Thus the original excursion is being propagated each switching cycle. Whether or not there are subharmonic oscillations depends on whether this propagation is converging or diverging. The difference in the inductor current from one cycle to the next (ΔI_n) is a function of S_n, S_f, and S_e, as follows:

$$\Delta I_n = \frac{S_f - S_e}{S_n + S_e} \Delta I_{n-1}$$

Hence, if the quantity $(S_f - S_e)/(S_n + S_e)$ is greater than 1, the inductor current diverges and subharmonic oscillations result. Notice that as S_e increases, the factor decreases. Also, when

the duty cycle is greater than 50%, and as the inductance decreases, the factor increases.

The LM3487 internally generates enough slope compensation S_e to allow for the use of reasonable inductances. The height of the compensation slope ramp V_{SL} can be found in the *ELECTRICAL CHARACTERISTICS* section. The LM3487 incorporates a patented scheme to increase S_e if there is need to use a smaller inductor. With the use of a single resistor R_{SL}, S_e can be increased indefinitely. R_{SL} increases the compensation slope by the amount:

$$\Delta S_e = 50 \times 10^{-6} \times f_S \times R_{SL} \left(\frac{V}{\mu s}\right)$$

Therefore,

$$S_e = f_S (V_{SL} + 50 \times 10^{-6} \times R_{SL}) \left(\frac{V}{\mu s}\right)$$

When excursions of the inductor current are divergent, the current sensing control loop is unstable and produces a subharmonic oscillation in the inductor current. This oscillation is viewed as a resonance in the outer voltage control loop at half the switching frequency. In the inductor design section, calculations for minimum inductance and necessary slope resistance R_{SL} are carried out based on this resonant peaking.

SOFT-START/SHUTDOWN

The softstart time of the LM3487 is programmed by an external capacitor connected from the SS/$\overline{SD}$ pin to ground, as shown in *Figure 7*. When the input voltage is applied to the device, a 2µA current source charges the capacitor at a constant rate. When the capacitor develops 0.75V (typical), the LM3487 begins switching the power MOSFET at low duty cycles. The softstart period continues until the softstart capacitor reaches 2V. Therefore, the turn-on delay period between 0 - 0.75V is:

$$t_{DELAY} = C_{SS} \frac{0.75}{2 \times 10^{-6}} \text{ (sec)}$$

and the softstart period between 0.75V - 2V is:

$$t_{SS} = C_{SS} \frac{1.25}{2 \times 10^{-6}} \text{ (sec)}$$

The time from when voltage is applied to the LM3487 to when the output voltage reaches its target can be approximated as $t_{DELAY} + t_{SS}$. A minimum value of 2.2nF is recommended for Css. During softstart, both current limit and OVP are enabled. However, since the feedback reference voltage ramps up with softstart voltage, the OVP threshold will ramp up along with it.

The LM3487 will not start up if the output voltage is held above 200mV. If the slope resistor (Rsl) is used, the hysteretic threshold will be lowered and up to 100mA of pre-load may be required for startup.

The LM3487 may be disabled by pulling the voltage at the SS/$\overline{SD}$ pin below 0.7V (typical). In this shutdown mode, the device consumes only 15µA (max). This is typically accomplished by presenting a low impedance path from the SS/$\overline{SD}$ pin to ground using a transistor as shown in *Figure 7*. Driving this impedance high will engage the softstart procedure and enable the device.

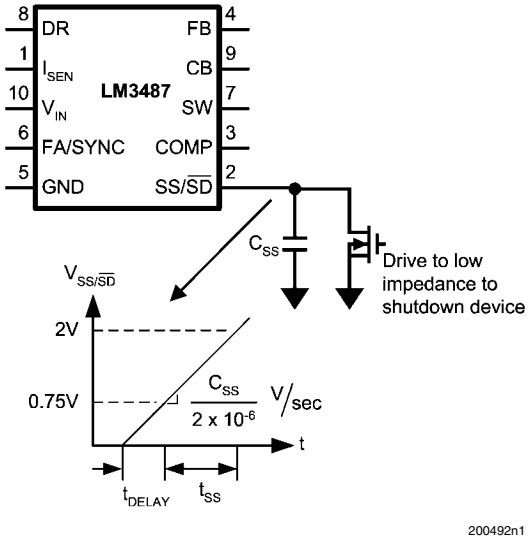


FIGURE 7. Soft Start Thresholds

INPUT UNDER VOLTAGE LOCKOUT (UVLO)

The input under voltage lockout, which is sensed at VIN, is set at 2.80V (typical). If the input voltage falls below this threshold, the FET will be turned off and the soft-start capacitor will be discharged. As the input voltage rises above 3.0V (typical) the LM3487 will restart from the soft-start phase.

CURRENT LIMIT PROTECTION

Current limit is sensed as the voltage across the sense resistor. When this voltage exceeds the V_{CL} threshold, current limit is activated and the LM3487 will immediately shut off the FET until the next cycle. This will cause the duty cycle and output voltage to drop. The current limit threshold can be adjusted using the sense resistor (see the *SETTING CURRENT LIMIT* section). In current limit operation, the FET will turn on each cycle and will remain on during the leading edge minimum on time (130nsec typical). During this minimum on time, inductor current may become excessive under short circuit conditions. In this case, a secondary current limit, Short Circuit Protection, is enabled.

SHORT CIRCUIT PROTECTION

When the voltage across the sense resistor (measured as the VIN – ISEN differential voltage) exceeds V_{SC}, short-circuit current limit gets activated. In the short-circuit protection mode, the external MOSFET is turned off. When the short is removed, the external MOSFET is held off for up to four cycles before resuming normal operation. The short circuit protection voltage V_{SC} is specified in the *ELECTRICAL CHARACTERISTICS* section.

Design Section

GENERAL

Power supply design involves making tradeoffs. The LM3487 provides many degrees of flexibility in choosing external components to accommodate various performance/component selection optimizations. For example, the internal slope compensation can be externally increased to allow smaller inductances to be used. The design procedures that follow provide instruction on how to select the external components in a typical LM3487 buck circuit in continuous conduction mode, as well as aid in the optimization of performance and/or compo-

nent selection. See *Figure 8* for component reference and typical circuit. The LM3487 may also be designed to operate in discontinuous conduction mode.

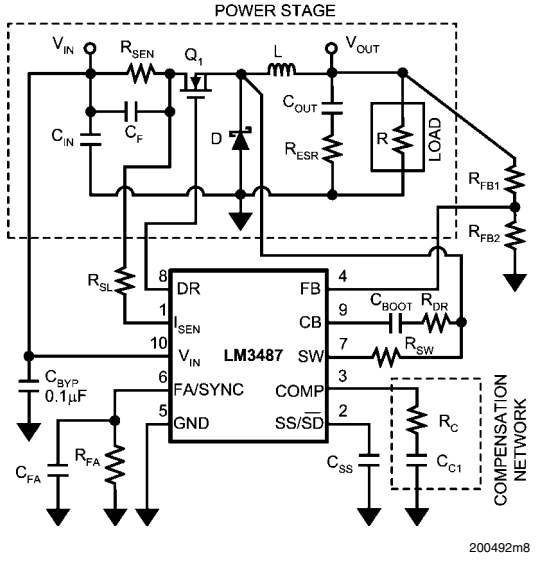


FIGURE 8. LM3487 Buck Converter Reference Schematic

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in *Figure 8*. The resistors are selected such that the voltage at the feedback pin is 1.26V. R_{FB1} and R_{FB2} can be selected using the equation:

$$V_{OUT} = 1.26*(1+ R_{FB1}/R_{FB2})$$

CALCULATING THE DUTY CYCLE

In buck converter applications, the duty cycle of the LM3487 may be calculated as:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_D - V_Q - V_{SEN}} \approx \frac{V_{OUT}}{V_{IN(MIN)}}$$

Where

V_D = forward drop of the power diode ≅ 0.5V

$V_Q = V_{DS}$ of the MOSFET when it is conducting ≅ $I_{OUT}*R_{DSON}$

V_{SEN} = Voltage across the sense resistor = I_{OUT} x R_{SEN}

This is the fraction of the switching period that the switch is on. The switch is off for the remainder of the period. This fraction is expressed as:

$$D' = 1 - D$$

The LM3487 has limits for the maximum and minimum duty cycle (see *ELECTRICAL CHARACTERISTICS*). The LM3487 can operate at 100% duty cycle, but only for a few periods (during transients). The gate voltage of the N channel MOSFET must be higher than V_{IN} in order for it to be on. The LM3487 provides this drive voltage through the voltage developed across C_{BOOT}, which is charged when the SW pin goes low (i.e. when the MOSFET is off and the diode is conducting). In this configuration, the drive voltage can not be maintained with a continuous 100% duty cycle. If the off time is too short to allow Cboot to recharge, the device will automatically shut down and enter softstart mode when V_{CBOOT} falls below approximately 1.5V. There is also a second level of protection, whereby if the FET stays on for more than typically 450µs, the LM3487 will restart regardless of the Cboot voltage. To avoid this condition, either decrease the duty cycle or lower the operating frequency.

The minimum duty cycle of the LM3487 corresponds to the minimum on time, or blank out time (see *ELECTRICAL CHARACTERISTICS*).

$$D_{MIN} = T_{MIN}* f_s$$

This will not limit how high the input voltage can rise, since the LM3487 will operate in hysteretic mode once the operating duty cycle decreases to the minimum duty cycle.

SETTING CURRENT LIMIT AND HYSTERETIC THRESHOLD

The current limit is the point at which the LM3487 begins to limit the peak switch current. The adjustable current limit of the LM3487 is set by the sense resistor R_{SN}. The voltage across R_{SN} is compared to an internal control voltage V_C. The onset of current limiting is when $V_{SEN(PEAK)}$ equals $V_{C(MAX)}$, or V_{CL} (current limit voltage). V_{SEN} is defined here as the differential voltage from the V_{IN} pin to the I_{SEN} pin. V_{CL} decreases as the duty cycle increases, as shown in *Figure 9*. Therefore, it is important to know both $V_{SEN(PEAK)}$ and $V_{CL(MIN)}$ at the maximum operating duty cycle, or lowest V_{IN} condition.

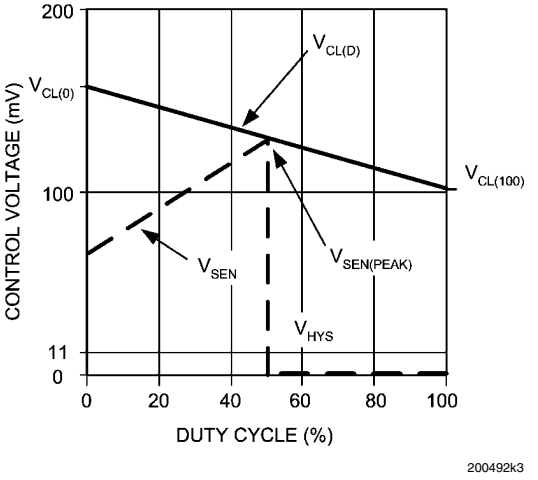


FIGURE 9. Current Limit and Hysteretic Threshold vs Duty Cycle

$$V_{SEN(PEAK)} = R_{SEN}(I_{OUT(MAX)} + \frac{V_{OUT}(1-D_{MAX})}{2 \times L \times f_S}) \text{ (V), } R_{SL} = 0$$

$$V_{CL(MIN)} = V_{CL(0)(MIN)} - D_{(MAX)} (V_{CL(0)(MIN)} - V_{CL(100)(MIN)})$$

where D_{MAX} is the duty cycle at the lowest V_{IN} condition.

To avoid current limit,

$$V_{SEN(PEAK)} < V_{CL(MIN)}$$

Therefore,

$$R_{SEN(MAX)} = \frac{V_{CL(0)(MIN)} - D_{MAX} (V_{CL(0)(MIN)} - V_{CL(100)(MIN)})}{I_{OUT(MAX)} + \frac{V_{OUT}(1-D_{MAX})}{2 \times L \times f_S}}$$

Example: $V_{IN(MIN)}$ = 4.5V, V_{OUT} = 2.5V, $I_{OUT(MAX)}$ = 3A, L = 3.3µH, f_s = 500kHz

$$R_{SEN(MAX)} = \frac{0.09 - 0.6\,(0.09 - 0.06)}{3 + \frac{2.5\,(1 - 0.6)}{2\,(500\ kHz)\,3.3\ \mu H}} = 0.022\Omega$$

Hysteretic threshold is the switch current at which the LM3487 enters the hysteretic mode of operation (see *OVER VOLTAGE PROTECTION* section). Hysteretic threshold is derived in a similar manner to current limit threshold, the only difference being that $V_{SEN(PEAK)}$ is compared $V_{C(MIN)}$ (V_{HYS}). Notice that V_{HYS} does not vary with the duty cycle. The hysteretic threshold is predetermined by the selection of R_{SN} above. The hysteretic threshold is:

$$I_{HYS} = \frac{V_{HYS}}{R_{SEN}} = \frac{0.011}{R_{SEN}}\ (A)$$

Continuing with the example above,

$$I_{HYS} = \frac{0.011}{0.02} = 0.55A$$

If the **peak switch current** decreases below this threshold, the LM3487 will operate in hysteretic mode (see *OVER VOLTAGE PROTECTION* section). In some designs, it will be desired to use R_{SL} so that lower valued inductors can be used (see *DEFAULT/ADJUSTABLE SLOPE COMPENSATION* section and Inductor section). Using R_{SL} will lower the current limit and the hysteretic threshold. See *Figure 10*. R_{SL} effectively adds an additional slope to the existing slope of the V_C waveform.

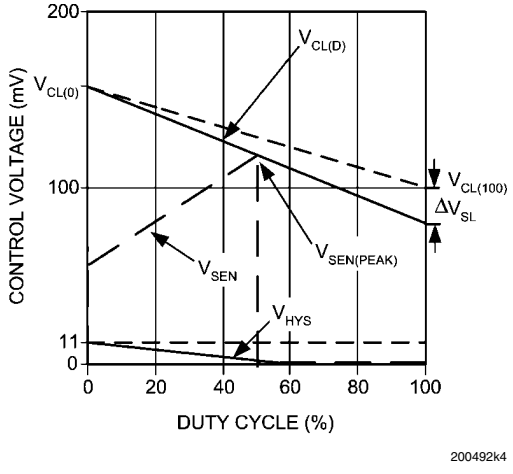


FIGURE 10. Current Limit and Hysteretic Threshold vs Duty Cycle with R_{SL}

When R_{SL} is used, the following equations apply:

$$R_{SEN(MAX)} = \frac{V_{CL(0)(MIN)} - D_{MAX}\,(V_{CL(0)(MIN)} - (V_{CL(100)(MIN)} - 50 \times 10^{-6} \times R_{SL}))}{I_{OUT} + \frac{V_{OUT}(1-D_{MAX})}{2 \times L \times f_S}}$$

$$I_{HYS} = \frac{MAX\,(V_{HYS} - 50 \times 10^{-6} \times R_{SL} \times D_{MAX},\ 0)}{R_{SEN}}\ (A)$$

where $MAX(V_{HYS} - 50x10^{-6} \times R_{SL} \times D_{MAX}, 0)$ is the larger of the two values in the parenthesis. R_{SL} can be used creatively to intentionally lower the hysteretic threshold, allowing for better performance at lower loads. However, when R_{SL} is used, there may be a minimum load requirement (see *START-UP/SOFT-START* section).

POWER INDUCTOR SECTION

1. Select Inductor Value

The LM3487 operates at high switching frequencies up to 1.4 MHz, which allows the use of small inductors. As the switching frequency (fs) increases, the inductance required for a given output voltage ripple decreases. This is made apparent in the following set of equations used to calculate the output voltage ripple.

$$\Delta V_{OUT(Pk\text{-}Pk)} \cong \Delta i_{L(Pk\text{-}Pk)} \times R_{ESR}\ (V)$$

$$\Delta i_{L(Pk\text{-}Pk)} = \frac{V_{OUT}\,(1-D)}{L \times f_S}\ (A)$$

Use the equations above for ΔV_{OUT} and Δi_L to select an inductance value.

The maximum voltage ripple in steady-state, PWM operation can be controlled by limiting Δi_L which in turn is set by the inductance value. Alternatively, one can simply choose Δi_L as a percentage of the maximum output current. Clearly, the size of the output capacitor ESR, R_{ESR}, will have an affect on which criteria is used to choose the inductance. When the ESR is relatively low (less than 100mΩ), such as in ceramic, OS-CON, and some low ESR tantalum capacitors, it is convenient to choose the inductance based on setting Δi_L to 30% of Iout (max). If the ESR is high, then it may be necessary to restrict Δi_L to a lower value so that the output voltage ripple is not too high. Generally speaking, the former suggestion of setting Δi_L to 30% of $I_{OUT(MAX)}$ is recommended.

2. Verify Stability

The inductance also affects the stability of the converter. The slopes S_n and S_f in *Figure 6* are functions of the inductance, while the compensation ramp, S_e, is fixed by default. Therefore if the inductance is too small, the converter may experience sub-harmonic oscillations. The LM3487 provides sufficient internal slope compensation to allow for inductances chosen according to the $\Delta i_L = 0.3 \times I_{OUT}$ guideline in most cases. Still, one should check to make sure the inductance is not too low before continuing the design process. If it is found that the selected inductance is too low, a patented scheme to increase the compensation ramp, S_e, is provided in the LM3487 (see *DEFAULT/ADJUSTABLE SLOPE COMPENSATION* section). In the calculations that follow, if it is found that the chosen inductance is too small, R_{SL} can be used to increase so that the inductance can be used.

In a current mode control architecture, there is an inherent resonance at half the switching frequency (see *DEFAULT/ADJUSTABLE SLOPE COMPENSATION* section). A convenient indicator of how much resonance exists is the quality factor Q. If Q is too high, subharmonic oscillations could occur, if Q is too low, the current mode architecture begins to act like a voltage mode architecture and the necessary compensation becomes more complex. This is discussed in more detail in the *COMPENSATION* section, but here it is important to calculate Q to be sure the selected inductance will not

cause problems to the stability of the converter. The calculations below call for an inductance that results in Q between 0.15 and 2. See the *COMPENSATION* section if the chosen inductance enforces Q to be out of this range. By default, no extra slope compensation is needed, so R_{SL} = 0. In general, a Q between 0.5 and 1 is optimal.

$$Q_{MAX} = \frac{1}{\pi\,(m_c \times D'_{(MIN)} - 0.5)}$$

Where,

$$D' = 1 - D$$

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_D - V_Q - V_{SEN}} \approx \frac{V_{OUT}}{V_{IN(MIN)}}$$

$$m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{f_S L (V_{SL} + 50 \times 10^{-6} \times R_{SL})}{1.8 R_{SEN} V_{IN(MIN)} D'_{(MIN)}}$$

$V_Q = V_{DS}$ of the MOSFET when it is conducting $I_{OUT}{}^* R_{DS(ON)}$.
V_{SEN} = Voltage across the sense resistor ≅ $I_{OUT} \times R_{SN}$
Back solving for L gives a range for acceptable inductances based on a range for Q:

$$\frac{V_{IN(MIN)} 1.8 R_{SEN} \left(\frac{1}{\pi Q_{MAX}} + D - 0.5\right)}{f_S (V_{SL} + 50 \times 10^{-6} \times R_{SL})} \le L \le \frac{V_{IN(MIN)} R_{SN} \left(\frac{1}{\pi Q_{MIN}} + D - 0.5\right)}{f_S (V_{SL} + 50 \times 10^{-6} \times R_{SL})}$$

It is recommended that:

Q(max) = 2, and

Q(min) = 0.15

Values for V_{SL} can be found in the *ELECTRICAL CHARACTERISTICS* section.

Note: Adding slope compensation with R_{SL} will decrease the current limit. An iterative process may be needed to meet current limit and stability requirements, see *PROGRAMMING CURRENT LIMIT/HYSTERETIC THRESHOLD* section.

OUTPUT CAPACITANCE SELECTION

A capacitance between 47µF - 100µF is typically used. Skip to "Calculations for the Output Capacitance" for minimum capacitance calculations.

Type of output capacitors

Different type of capacitors often have different combinations of capacitance, equivalent series resistance (ESR), and voltage ratings. High-capacitance multi-layer ceramic capacitors (MLCCs) have a very low ESR, typically 12mΩ, but also relatively low capacitance and low voltage ratings. Tantalum capacitors can have fairly low ESR, such as 18mΩ, and high capacitance (up to 1mF) at higher voltage ratings than MLCCs. Aluminum capacitors offer high capacitance and relatively low ESR and are available in high voltage ratings. OSCON capacitors can achieve ESR values that are even lower than those of MLCCs and with higher capacitance, but the voltage ratings are low. Other tradeoffs in capacitor technology include temperature stability, surge current capability, and capacitance density (physical size vs. capacitance).

Output Capacitor Considerations

Skip to the "Calculations for the output capacitor" subsection if a quick design is desired. While it is generally desired to use as little output capacitance as possible to keep costs down, the output capacitor should be chosen with care as it directly affects the ripple component of the output voltage as well as other components in the design. The output voltage ripple is directly proportional to the ESR of the output capacitor (see *POWER INDUCTOR* section). Therefore, designs requiring low output voltage ripple should have an output capacitor with low ESR. Choosing a capacitor with low ESR has the additional benefit of requiring one less component in the compensation network, as discussed in the Compensation section.

In addition to the output voltage ripple, the output capacitor directly affects the output voltage overshoot in a load transient. Two transients are possible: an unloading transient and a loading transient. An unloading transient occurs when the load current transitions to a higher current, and charge is unloaded from the output capacitor. A loading transient is when the load transitions to a lower current, and charge is loaded to the output capacitor. How the output voltage reacts during these transitions is known as the transient response. Both the capacitance and the ESR of the output capacitor will affect the transient response.

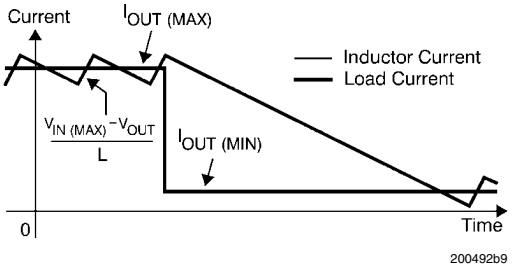


FIGURE 11. A Loading Transient

The control loop of the LM3487 can be made fast enough to saturate the duty cycle when the worst case lode transient occurs. This means the duty cycle jumps to D_{MIN} or D_{MAX}, depending on the type of load transient. In a loading transient, as shown in *Figure 11*, the duty cycle drops to D_{MIN} while the inductor current falls to match the load current. During this time, the regulator is heavily dependent on the output capacitors to handle the load transient. The initial overshoot is caused by the ESR of the output capacitors. How the output voltage recovers after that initial excursion depends on how fast the inductor current falls and how large the output capacitance is. See *Figure 12*.

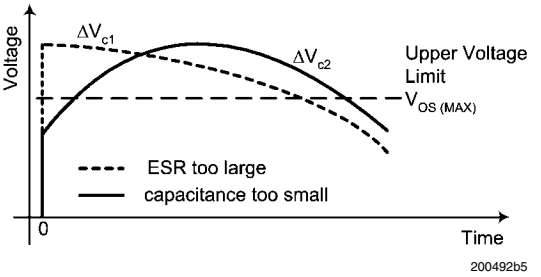


FIGURE 12. Output Voltage Overshoot Violation

The ESR and the capacitance of the output capacitor must be carefully chosen so that the output voltage overshoot is within

the design's specification $V_{OS(MAX)}$. If the total combined ESR of the output capacitors is not low enough, the initial output voltage excursion will violate the specification, see ΔV_{C1}. If the ESR is low enough, but there is not enough output capacitance, the output voltage will travel outside the specification window due to the extra charge being dumped into the capacitor, see ΔV_{C2}. The LM3487 has output over voltage protection (OVP) which could trigger if the transient overshoot is high enough. If this happens, the controller will operate in hysteretic mode (see *OVER VOLTAGE PROTECTION* section) for a few cycles before the output voltage settles to its steady state. If this behavior is not desired, substitute V_{OVP} (referred to the output) for $V_{OS(MAX)}$ (V_{OVP} is found in the *ELECTRICAL CHARACTERISTICS* table) to find the minimum capacitance and maximum ESR of the output capacitor.

Calculations for the Output Capacitor

During a loading transient, the delta output voltage ΔV_c has two changing components. One is the voltage difference across the ESR (ΔV_r), the other is the voltage difference caused by the gained charge (ΔV_q). This gives:

$$\Delta V_c = \Delta V_r + \Delta V_q$$

The design objective is to keep ΔV_c lower than some maximum overshoot ($V_{OS(MAX)}$). $V_{OS(MAX)}$ is chosen based on the output load requirements.

Both voltages ΔV_r and ΔV_qwill change with time. For ΔV_r the equation is:

$$\Delta V_r = R_{ESR}(\Delta I_{OUT(MAX)} - \frac{V_{OUT} - D_{MIN}V_{IN}}{L} t)(V)$$

where,

R_{ESR} = the output capacitor ESR

ΔI_{OUT} = the difference between the load current change $I_{OUT(MAX)} - I_{OUT(MIN)}$

D_{MIN} = Minimum duty cycle of device ($T_{MIN} \bullet f_s$)

Evaluating this equation at t = 0 gives $\Delta V_{r(max)}$. Substituting $V_{OS(MAX)}$ for $\Delta V_{r(MAX)}$ and solving for R_{ESR} gives:

$$R_{ESR(MAX)} = \frac{V_{OS(MAX)}}{\Delta I_{OUT(MAX)}} \Omega$$

The expression for ΔV_q is:

$$\Delta V_q = \frac{\Delta I_{OUT(MAX)}}{C_{OUT}} t - \frac{V_{OUT} - D_{MIN}V_{IN}}{2 X L X C_{OUT}} t^2 (V)$$

From *Figure 13* it can be seen that ΔV_C will reach its peak value at some point in time and then decrease. The larger the output capacitance is, the earlier the peak will occur. To find the peak position, let the derivative of ΔV_C go to zero, and the result is:

$$tpeak = \frac{\Delta I_{OUT(MAX)} x L}{V_{OUT} - D_{MIN}V_{IN}} - C_{OUT}R_{ESR}$$

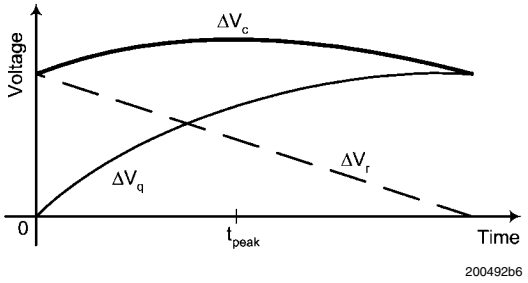


FIGURE 13. Output Voltage Overshoot Peak

The intention is to find the capacitance value that will yield, at t_{peak}, a ΔV_C that equals $V_{OS(max)}$. Substituting tpeak for t and equating ΔV_C to $V_{OS(max)}$ gives the following solution for $C_{OUT(MIN)}$:

$$C_{OUT(MIN)} = \frac{L\left(V_{OS(MAX)} - \sqrt{V_{OS(MAX)}^2 - (\Delta I_{OUT(MAX)} \times R_{ESR})^2}\right)}{(V_{OUT})\, R_{ESR}^2} (F)$$

The chosen output capacitance should not be less than 47µF, even if the solution for $C_{OUT(MIN)}$ is less than 47µF. Notice it is already assumed that the total ESR is no greater than $R_{ESR(MAX)}$, otherwise the term under the square root will be a negative number.

POWER MOSFET SELECTION

The drive pin of LM3487 must be connected to the gate of an external MOSFET. In a buck topology, the drain of the external N-Channel MOSFET is connected to the input and the source is connected to the inductor. The C_B pin voltage provides the gate drive needed for an external N-Channel MOSFET. The gate drive voltage depends on the input voltage (see *TYPICAL PERFORMANCE CHARACTERISTICS*). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub-logic level MOSFET should be used.

The selected MOSFET directly controls the efficiency. The critical parameters for selection of a MOSFET are:

1. Minimum threshold voltage, V_{TH}(MIN)
2. On-resistance, R_{DS}(ON)
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}
5. Maximum drain to source voltage, $V_{DS(MAX)}$
6. Maximum drain current, $I_{D(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the input voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the input voltage. Also, the I_D rating must be greater than the maximum peak load current.

The power losses in the MOSFET can be categorized into conduction losses and ac switching or transition losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, P_{COND}, is the I^2R loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND(MAX)} = I^2 D_{MAX}\left[1 + \frac{1}{12}\left(\frac{\Delta i_{(PK-PK)}}{I}\right)^2\right] R_{DS(ON)}$$

where D_{MAX} is the maximum operating duty cycle:

$$D_{max} \approx \frac{V_{OUT}}{V_{IN(MIN)}}$$

The turn-on and turn-off transition times of a MOSFET from the MOSFET specifications require tens of nano-seconds. C_{RSS} and Q_g are needed from the MOSFET specifications to estimate the large instantaneous power loss that occurs during these transitions.

The average amount of gate current required to turn the MOSFET on can be calculated using the formula:

$$I_G = Q_g.F_S$$

The required gate drive power to turn the MOSFET on is equal to the switching frequency times the energy required to deliver the charge to bring the gate charge voltage to V_{DR} (see *ELECTRICAL CHARACTERISTICS* and *TYPICAL PERFORMANCE CHARACTERISTICS* for the drive voltage specification).

$$P_{Drive} = F_S.Q_g.V_{DR}$$

It is sometimes helpful or necessary to slow down the turn on transition of the FET so that less switching noise appears at the I_{SEN} pin. This can be done by inserting a drive resistor R_{DR} in series with the boot-strap capacitor (see *Figure 8*). This can help reduce sensing noise that may be preventing designs from operating at or near the LM3487's minimum duty cycle limit. Gate drive resistors from 2.2Ω to 51Ω are recommended.

CALCULATING POWER DISSIPATION

Although most of the power loss in a switching regulator is dissipated in the FETs, it can also be useful to know the power used by the IC. The electrical characteristics table shows a typical value for Iq, however this does not include the FET drive current. The following equation gives an accurate estimate of power lost in the device during switching: Where I_G is the average drive current defined above, and V_{DR} is the FET drive voltage, typically 6.1V.

$$P_D = V_{in}I_q + (V_{in} - V_{DR})\, I_G$$

POWER DIODE SELECTION

The output current commutates through the diode when the external MOSFET turns off. The three most important parameters for the diode are the peak current, peak inverse voltage, and average power dissipation. Exceeding these ratings can cause damage to the diode. The average current through the diode is given by:

$$I_{D(AVG)} = I_{OUT} \text{ x } (1\text{-}D)$$

where D is the duty cycle and I_{OUT} is the output current. The diode must be rated to handle this current.

The off-state voltage across the diode in a buck converter is approximately equal to the input voltage. The peak inverse voltage rating of the diode must be greater than the off-state voltage of the diode. To improve efficiency, a low forward drop schottky diode is recommended.

INPUT CAPACITOR SELECTION

In a buck converter, the high side switch draws large ripple currents from the input capacitor. The input capacitor must be rated to handle this RMS current.

$$I_{RMS_CIN} = I_{OUT} \sqrt{\frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}}}$$

The power dissipated in the input capacitor is given by:

$P_{D(CIN)}=I_{RMS_CIN}^2 R_{ESR_CIN}$,

where R_{ESR_CIN} is the ESR of the input capacitor. The input capacitor must be selected to handle the rms current and must be able to dissipate the power. $P_{D(CIN)}$ must be lower than the rated power dissipation of the selected input capacitor. In many cases, several capacitors have to be paralleled to handle the rms current. In that case, the power dissipated in each capacitor is given by:

$P_{D(CIN)} = (I^2_{RMS_CIN}R_{ESR_CIN})/n^2$, where n is the total number of capacitors paralleled at the input.

A 0.1µF or 1µF ceramic bypass capacitor is also recommended on the V_{IN} pin of the IC. This capacitor must be connected very close to the pin.

COMPENSATION

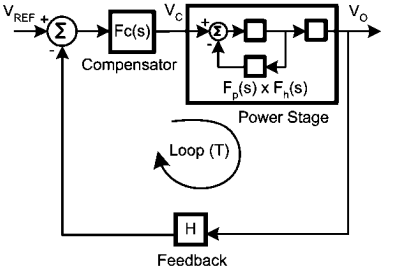


FIGURE 14. Control Block Diagram of a Current Mode Controlled Buck Converter

The LM3487 is a current mode controller, therefore the control block diagram representation involves 2 feedback loops (see *Figure 14*). The inner feedback loop derives its feedback from the sensed inductor current, while the outer loop monitors the output voltage. This section will not give a rigorous analysis of current mode control, but rather a simplified but accurate method to determine the compensation network. The first part reveals the results of the model, giving expressions for solving for component values in the compensation network.

The compensation network is designed around the power components, or the power stage. An isolated schematic of the error amplifier and the various compensation components is shown in *Figure 15*. The error amplifier in conjunction with the compensation network makes up the compensator block in *Figure 14*. The purpose of the compensator block is to stabilize the control loop and achieve high performance in terms of the transient response, audio susceptibility and output impedance.

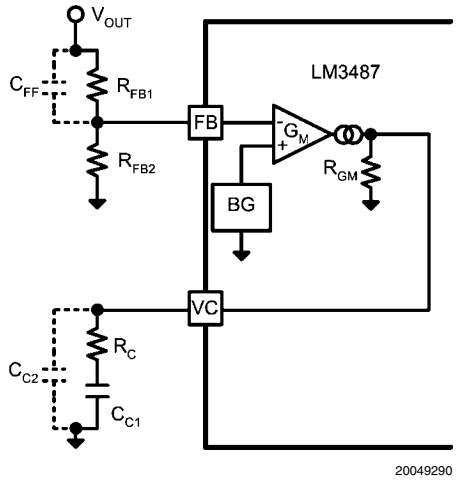


FIGURE 15. LM3487 Compensation Components

Figure 16 shows a bode plot of a typical current mode buck regulator. It is an estimate of the actual plot using the asymptotic approach. The three plots shown are of the compensator, powerstage, and loop gain, which is the product of the power stage, compensator, and feedback gain. The loop gain determines both static and dynamic performance of the converter. The power stage response is fixed by the selection of the power components, therefore the compensator is designed around the powerstage response to achieve a good loop response. Specifically, the compensator is added to increase low frequency magnitude, extend the 0dB frequency (crossover frequency), and improve the phase characteristic.

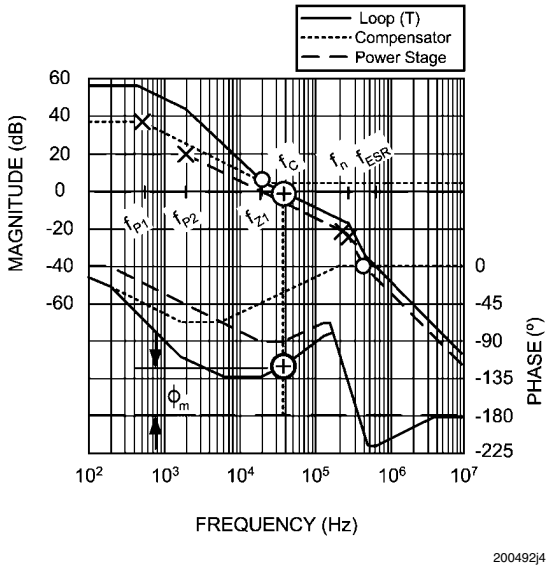


FIGURE 16. Typical Loop, Compensator, and Power Stage Bode Plots for LM3487 Buck Circuits. Poles, Zeros and Important Measurements are Labeled

There are several different types of compensation that can be used to improve the frequency response of the control loop. To determine which compensation scheme to use, some information about the power stage is needed.

Use $V_{IN} = V_{IN(MIN)}$ and $R = R_{MIN}$ ($I_{OUT(MAX)}$) when calculating compensation components.

$$H = \text{feedback gain} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

$$A_{DC} = \frac{R}{1.8R_{SEN}} \frac{1}{1 + \frac{R}{f_S L}\left[m_c \times D' - 0.5\right]}$$

$$m_c = 1 + \frac{S_e}{S_n}$$

$$S_e = f_S(V_{SL} + 50\text{x}10^{-6}\, R_{SL})$$

$$S_n = \frac{V_{IN}D' \times 1.8R_{SEN}}{L}$$

$$f_{p1} = \frac{1}{2\pi}\left[\frac{1}{C_{OUT}R} + \frac{1}{f_s L C_{OUT}}(m_c \times D' - 0.5)\right](\text{Hz})$$

$$f_{ESR} = \frac{1}{2\pi C_{OUT}R_{ESR}}(\text{Hz})$$

$$Q_{MAX} = \frac{1}{\pi\,(m_c \times D'_{(MIN)} - 0.5)}$$

With the power stage known, a compensator can be designed to achieve improved performance and stability. The LM3487 will typically require only a single resistor and capacitor for compensation, but depending on the power stage it could require three or four external components.

It is a good idea to check that Q is between 0.15 and 2, if it was not already done when selecting the inductor. If Q is less than 0.15 or greater than 2, skip to the *SAMPLING POLE QUALITY FACTOR* section below before continuing with the compensator design.

First, a target crossover frequency (f_c) for the loop gain must be selected. The crossover frequency is the bandwidth of the converter. A higher bandwidth generally corresponds to faster response times and lower overshoots to load transients. However, the bandwidth should not be much higher than 1/10 the switching frequency.

The schematic of the LM3487 compensator is shown in *Figure 15*. The default design uses R_c and C_{C1} to form a lag (type 2) compensator. The C_{C2} capacitor can be added to form an additional pole that is typically used to cancel out the ESR zero of the output capacitor. Finally, if extra phase margin is needed, the Cff capacitor can be added (this does not help at low output voltages, see below).

The strategy taken here for choosing R_c and C_{C1} is to set the crossover frequency with R_c, and set the compensator zero with C_{C1}. Using the selected target crossover frequency, f_C, set R_C to:

$$R_C = \frac{f_C \times R_{GM}}{A_{DC} \times GM \times R_{GM} \times H \times f_{P1} - f_C}\,\Omega$$

f_C = Crossover frequency in Hertz ($f_S/20$ - $f_S/10$ is recommended)

$R_{GM} = 50x10^3\Omega$

$GM = 1000x10^{-6}$ A/V

The compensator zero, f_{Z1}, is set with C_{C1}. When fast transient responses are desired, f_{Z1} should be placed as high as possible, however it should not be higher than the selected crossover frequency f_C. The guideline proposed here is to choose C_{C1} such that f_{Z1} falls somewhere between the power pole f_{P1} and ½ decade before the selected crossover frequency:

$$\frac{3.16}{2\pi f_C R_C} \leq C_{C1} \leq \frac{1}{2\pi f_{p1} R_C}$$

In this compensation scheme, the pole created by C_{C2} is used to cancel out the zero created by the ESR of the output capacitor. In other schemes such as the methods discussed in the *SAMPLING POLE QUALITY FACTOR* subsection, the ESR zero is used. For the typical case, use C_{C2} if:

$$f_{ESR} < \frac{f_s}{2}$$

$$C_{C2} = \frac{R_{GM} + R_C}{2\pi f_{ESR} R_{GM} R_C} (F)$$

PLOTTING THE OPEN LOOP RESPONSE

The open loop response is expressed as:

$T = A_{DC} \times A_{CM} \times H \times F_p(s) \times F_c(s)$

Where A_{DC} and H are given above and

$A_{CM} = GM \times R_{GM}$

$$F_{P(S)} = \frac{1 + \frac{s}{2\pi f_{ESR}}}{1 + \frac{s}{2\pi f_{p1}}} F_{h(S)}$$

$$F_h(s) = \frac{1}{s^2\left(\frac{1}{\pi f_s}\right)^2 + s\left(\frac{1}{\pi f_s Q}\right) + 1}$$

$$F_C(s) = \frac{(sC_{C1}R_C + 1)}{sC_{C1}(R_{GM} + R_C) + 1}, C_{C2} \text{ not used}$$

$$F_C(s) = \frac{(sC_{C1}R_C + 1)}{s^2 C_{C1}C_{C2}R_C R_{GM} + s(C_{C2}R_{GM} + C_{C1}(R_{GM} + R_C)) + 1}, C_{C2} \text{ used}$$

One can plot the magnitude and phase of the open loop response to analyze the frequency response.

Example: Compensation Design

$4.5V \leq V_{IN} \leq 5.5V$

$V_{OUT} = 2.5V$

$I_{OUT} = 3A$ ($R = 0.83\Omega$)

$R_{SEN} = 0.02\Omega$

$L = 3.3\mu H$

$R_{SL} = 0\Omega$

$C_{OUT} = 100\mu F$

$R_{ESR} = 0.01\Omega$

$f_s = 500kHz$

First, calculate the power stage parameters using $V_{IN(MIN)}$ and $R_{(MIN)}$:

$$H = \text{feedback gain} = \frac{1.27}{2.5} = 0.508$$

$$A_{DC} = \frac{0.83}{(1.8)\,0.02} \frac{1}{1 + \frac{0.83}{(500 \times 10^3)(3.3 \times 10^{-6})}[(2.49)(0.44) - 0.5]} = 17.7$$

$$f_{p1} = \frac{1}{2\pi}\left(\frac{1}{(100 \times 10^{-6})(0.83)} + \frac{1}{(500 \times 10^3)(3.3 \times 10^{-6})(100 \times 10^{-6})}\right.$$
$$\left.[(2.49)(0.44) - 0.5]\right) = 2.49 \text{ kHz}$$

$$f_{ESR} = \frac{1}{2\pi(100 \times 10^{-6})(0.01)} = 159kHz$$

$$Q = \frac{1}{\pi[(2.49)(0.44) - 0.5]} = 0.53$$

In this example, a crossover frequency of 20kHz is chosen, so: $f_C = 20000$. R_C is now calculated using the power stage information and the target crossover frequency f_C:

$$R_C = \frac{(20 \times 10^3)(50 \times 10^3)}{(17.7)(0.001)(50 \times 10^3)(0.508)(2.49 \times 10^3) - (20 \times 10^3)}$$
$$= 910\Omega$$

Selecting $R_C = 910\Omega$ sets the high frequency gain of the compensator such that a crossover frequency of f_C is obtained. The capacitor C_{C1} sets the compensator zero, f_{Z2}. Set f_{Z2} between the power pole f_{P1} and ½ decade before the target crossover frequency f_C:

$$\frac{3.16}{2\pi(20 \times 10^3)(910)} \leq C_{C1} \leq \frac{1}{2\pi(2.49 \times 10^3)(910)}$$

$$28 \text{ nF} \leq C_{C1} \leq 70 \text{ nF}$$

Choosing $C_{C1} = 70nF$ will set $f_{Z2} = f_{P1}$, canceling out the power pole and insuring a –20dB/decade slope in the low frequency

magnitude response. In other words, the phase margin below the crossover frequency will always be higher than the phase margin at the crossover frequency.

If better transient response times are desired, set f_{z2} closer to 1/2 decade before fc (smaller capacitor). This trades more low frequency gain for less phase margin, which translates to faster but more oscillatory step responses. We pick C_{C1} = 47nF.

If the esr zero of the output capacitor (f_{ESR}) is too low or if more phase margin is required, additional components may be added to increase the flexibility of the compensator.

Use C_{C2} if $f_{ESR} < ½\ f_S$, that is if:

$$\frac{1}{2\pi C_{OUT} R_{ESR}} < 250kHz$$

For this example, f_{ESR} = 159 kHz, so use C_{C2}.

$$C_{C2} = \frac{50 \times 10^3 + 910}{2\pi\ (159 \times 10^3)\ (50 \times 10^3)\ 910} = 1.1\ nF$$

In general, Cc2 should be kept as small as possible to prevent the gain and phase margins from dropping too low.

The equations used here for R_C, C_{C1}, and C_{C2} are approximations valid when $C_{C2} << C_{C1}$. For exact equations, see Plotting Open Loop Response earlier in this section. In some cases, the desired inductance is several times higher than the optimal inductance set by the internal slope compensation. This results in a Q lower than 0.15, in which case additional methods of compensating are presented (see *SAMPLING POLE QUALITY FACTOR* section).

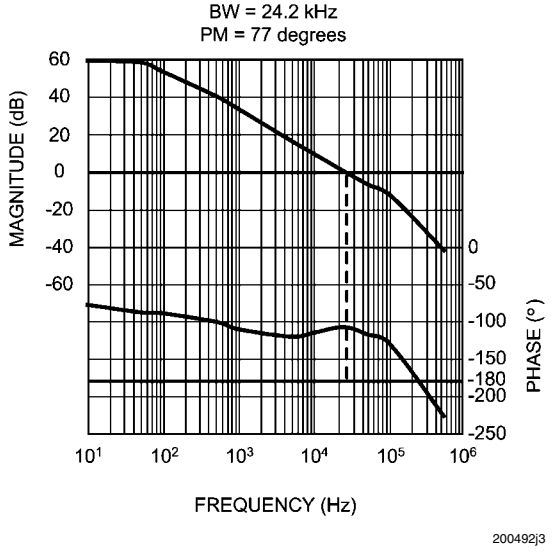


FIGURE 17. Open Loop Frequency Response for LM3487 Compensation Design Example

SAMPLING POLE QUALITY FACTOR

In a current mode control architecture, there is an inherent resonance at half the switching frequency. The LM3487 internally compensates for this by adding a negative slope to the PWM control waveform (see *DEFAULT/ADJUSTABLE SLOPE COMPENSATION* section). The factor in the power stage equations above, Q, describes how much resonance will be observed. Q is a function of duty cycle and m_c. *Figure 18* shows how the power stage bode plot is affected as Q is varied from 0.01 to 10. The resonance is caused by two complex poles at half the switching frequency. If m_c is too low, the resonant peaking could become severe coinciding with subharmonic oscillations in the inductor current. If m_c is too high, the two complex poles split and the converter begins to act like a voltage mode converter and the compensation scheme used above should be changed.

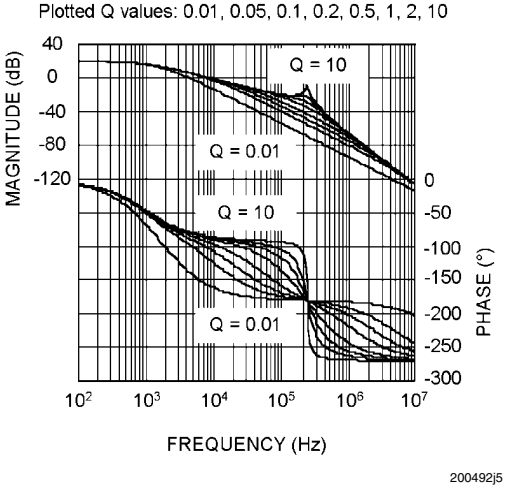


FIGURE 18. The Quality Factor Q of the Two Complex Poles is used to qualify how much resonant peaking is observed in the Power Stage Bode Plot

If Q>2, the sampling poles are imaginary and are approaching the right half of the imaginary plane (the system is becoming unstable). In this case, Q must be decreased by either increasing the inductance, or more preferably, adding more slope compensation through the R_{SL} resistor (see *DEFAULT/ADJUSTABLE SLOPE COMPENSATION* section).

If Q<0.15, it means that one of the sampling poles is decreasing in frequency towards the dominant power pole, f_{p1}. There are three ways to compensate for this. Decrease the crossover frequency, add a phase lead network, or use the output capacitor's ESR to cancel out the low frequency sampling pole.

One option is to decrease the crossover frequency so that the phase margin is not as severely decreased by the sampling pole. Decreasing the crossover frequency to between 1kHz to 10kHz is advisable here. As a result, there will be a decrease in transient response performance.

Another option is the use of the feed-forward capacitor, Cff (see *Figure 15*. This will provide a positive phase shift (lead) which can be used to increase phase margin. However, it is important to note that the effectiveness of Cff decreases with output voltage. This is due to the fact that the frequencies of the zero f_{zff} and pole f_{pff} get closer together as the output voltage is reduced.

The frequency of the feed-forward zero and pole are:

$$f_{zff} = \frac{1}{2\pi R_{FB1} C_{ff}}\ (Hz)$$

$$f_{pff} = \frac{1}{2\pi R_{FB1} C_{ff}} \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = f_{zff} \frac{V_{OUT}}{V_{FB}}\ (Hz)$$

A third option is to strategically place the ESR zero f_{ESR} of the output capacitor to cancel out the sampling pole. In this case, the capacitor C_{C2} will not be used to cancel out f_{ESR}. f_{ESR} should be placed around the crossover frequency f_c, but this will depend on how low Q is.

CURRENT SENSE FILTERING AND LAYOUT

High side current sensing like that used in the LM3487 buck circuit is subject to high frequency noise at the turn on of the MOSFET. The noise will appear in the current sense signal and could cause duty cycle jittering. This will produce undesirable spectrum noise. The LM3487 uses a 130 ns blanking time at the beginning of every cycle to ignore this noise, but the noise may be prevalent after the blanking time. Because the noise spike increases with input voltage and load current, duty cycle jitter occurs more commonly at input voltages above 15V and loads above 2A. Current sense filtering is necessary to reduce the noise at the I_{SEN} pin and stabilize the jitter.

The schematic in *Figure 19* shows the current sense circuit with the recommended RC filter. The layout of the filter components is very important. Grounding should be very good for the input bypass capacitor, and the components at the Vin node should be kept very close together. An example layout is shown in *Figure 19*. The better the layout, the less delay necessary in the RC filter. The RC time constant of the filter should be in the range of 10ns to 300ns. The resistor in the RC filter should be less than 100 ohm to avoid adding appreciable slope compensation.

It is important to keep the RC time constant at a minimum because the delay of the filter has a side effect of increasing the hysteretic threshold current (see *PROGRAMMING THE CURRENT LIMIT/HYSTERETIC THRESHOLD* section).

When creating a PCB layout, a few important guidelines should be followed. First, the switch node should be kept as small as possible. Also, the catch diode, input capacitors, and output capacitors should be grounded to a large ground plane, with the input cap grounded at a point close to the catch diode anode. Keeping the feedback trace short and away from the inductor is also important. See Application Note AN-1229 for more specific information regarding PCB layout.

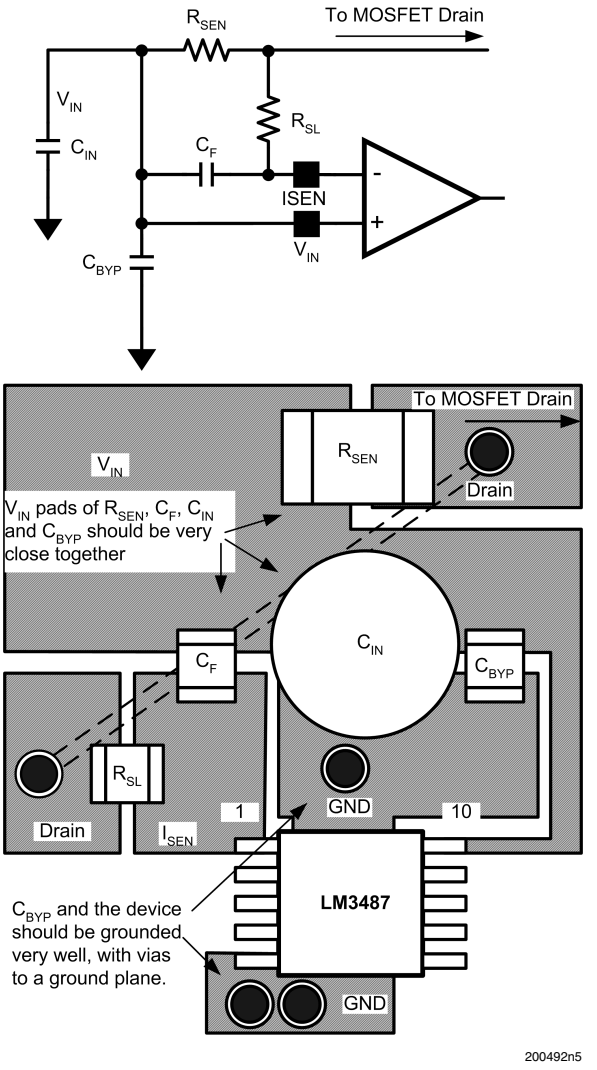
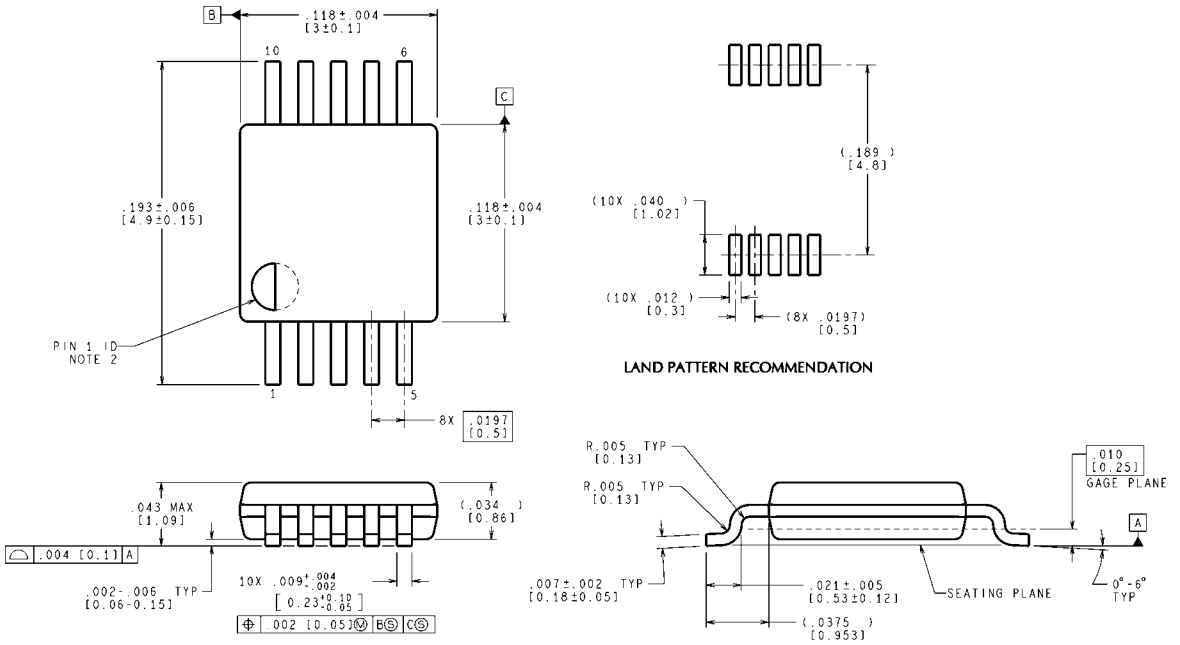


FIGURE 19. Current Sense Filter Schematic and Local Layout Recommendation

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

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